REMARKS

Claims 108-121 remain pending.

The Examiner rejected claims 108, 109 and 114-117 under 35 U.S.C. U.S.C. §103(a) as being unpatentable over Satya et al. (US 5,959,459) in view of Chiang et al. (US 6,309,956) and Munakata (Japanese Patent No. 02-087544). Additionally, claims 110, 112, 113, 118, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al. and Chiang et al., and in view of Munakata and further in view of Huang et al. (US 6,001,733). Claims 111, 119, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al., Chiang et al., and Munakata in view of Huang et al., and further in view of Bennett (US 3,861,023). The Examiner's rejections are respectfully traversed as follows.

Claim 108 is directed towards a "method of fabricating a semiconductor die." Claim 1 also requires "forming a test structure on the semiconductor die, wherein at least a portion of the test structure includes a dummy structure in a top conductive layer, wherein the dummy structure of the test structure serves as both a dummy structure and a part of a voltage contrast structure." Since the dummy structure of the test structure serves as both a dummy structure and a part of a voltage contrast structure, the test structure as a whole can be said to serve as both a dummy structure and a voltage contrast structure. Thus, claim 108 also requires "performing voltage contrast testing on the test structure that serves as both a dummy structure and a voltage contrast structure to detect electrical defects within the test structure."

Claim 108 also defines serving as a dummy structure as "the dummy structure of the test structure being part of a plurality of dummy structures that are distributed within empty spaces of the semiconductor die to facilitate an even polishing of a surface of the semiconductor die". This amendment is supported on page 44, lines 1 and 14-15, among other places. Claim 108 further recites that "wherein only a portion of the dummy structures each serve as a voltage contrast structure while the other portion of dummy structures do not each serve as a voltage contrast structure". This amendment is supported on page 44, lines 24-26, among other places, which specifies that only *some* of the dummy structures are used for voltage contrast testing. In other words, the dummy structure of the test structure serves as both a dummy structure and a part of a voltage contrast structure, while at least one of the other dummy structures serves as a dummy structure to facilitate even polishing but does not serve as part of a voltage contrast structure.

The Satya et al. reference is directed towards test structures and methods of performing voltage contrast testing on such VC test structures. The Chiang et al. reference generally teaches

how dummy structures can be used along with a low k dielectric to result in a more stable active interconnect structure.

The Examiner is reminded that although Satya teaches voltage contrast (VC) structures and Chiang teaches dummy structures, it is respectfully submitted that these two features cannot be combined since Satya teaches away from using its VC structures as dummy structures as defined in the claimed invention. In the claimed invention, dummy structures are defined as being distributed within the empty spaces of the semiconductor die to facilitate an even polishing of a surface of the semiconductor die. In contrast to dummy structures of the claimed invention, the VC structures of Satya are clearly placed in a separate area than the empty spaces of the semiconductor die. See Column 1, Lines 29-40 (Emphasis added): "These defect monitors are typically constructed at the same time but *in a different chip location* on the semiconductor substrate than the product VLSI devices, and are discarded once the useful defect information is extracted." See also Column 3, Lines 43-45: a variety of monitor structures are fabricated *in the dicing-kerf regions* or as a distinct test chip on the semiconductor wafer." Additionally, the VC structures of Satya are composed of large structure array chains which would not easily fit within a dummy area of the active region. See Fig. 1 and 2.

Since Satya's VC structure's are placed in locations that are not suitable for dummy structures (*e.g.*, in the scribe line or on a separate test chip), Satya teaches away from forming dummy structures as defined in the claimed invention within its VC structures since dummy structures in the manner claimed are necessarily formed in empty regions within the semiconductor die and, thus, dummy structures cannot be added to the VC structures of Satya which are not located in such empty regions. In other words, the VC structures of Satya cannot fulfill the purpose of dummy structures, which is to facilitate even polishing during CMP, since the VC structures of Satya are not located in empty spaces of the active region. Accordingly, one would not be motivated to add dummy structures to the VC structures of Satya to alleviate these CMP problems since addition of such dummy structures to the VC structures of Satya would not achieve this goal.

It is respectfully submitted that there is no motivation to combine the VC structure teachings of Satya with the dummy structure teachings of Chiang.

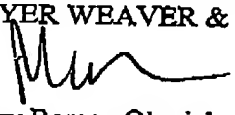
The secondary reference Munakata generally teaches a dummy wiring circuit that is used to "evaluate the quality and reliability of wiring on the semiconductor circuit". See translated abstract. However, it is respectfully submitted that Munakata does not appear to teach that these dummy structures also serve to facilitate even polishing by being distributed in the empty spaces of the semiconductor die, in the manner claimed. Thus, although Munakata teaches a dummy

test structure that is used to evaluate wiring in a semiconductor circuit, Munakata fails to teach or suggest a test structure that includes a dummy structure that serves as both a dummy structure that facilitates even polishing of the die surface and as part of a voltage contrast structure, in the manner claimed.

For the forgoing reasons, it is respectfully submitted that claim 108 is patentable over the cited references. The Examiner's rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 109-121 each depend directly or indirectly from independent claim 108 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claim 108. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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